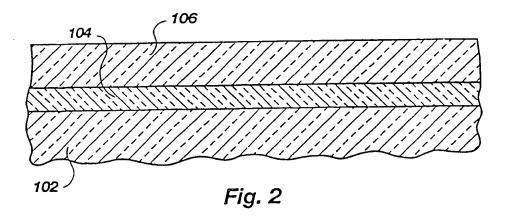


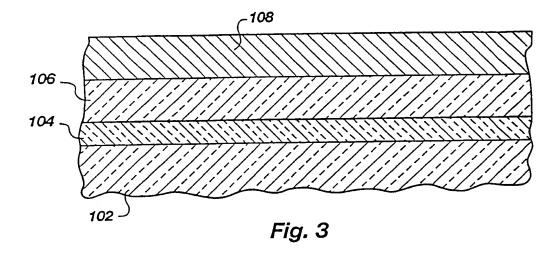
Fig. 1

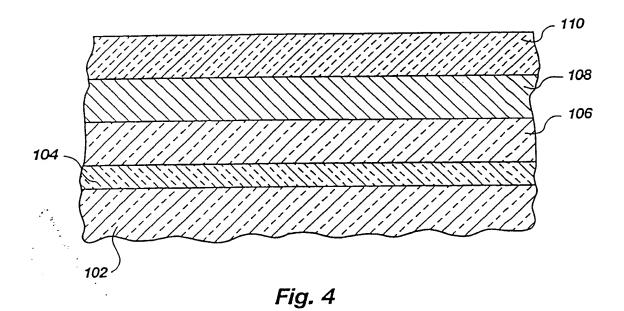


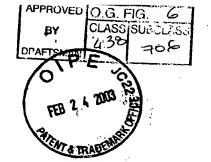


TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON SUBSTRATE DURING GATE STACK ET

Inventor: Pan et al. Serial No.: 09/614,113 Docket No.: 2269-2915.3US







TITLE: TECIINIQUE FOR ELIMINATION OF PITTING ON SILICON SUBSTRATE DURING GATE STACK For Inventor: Pan et al.

Serial No.: 09/614,113

Docket No.: 2269-2915.3US

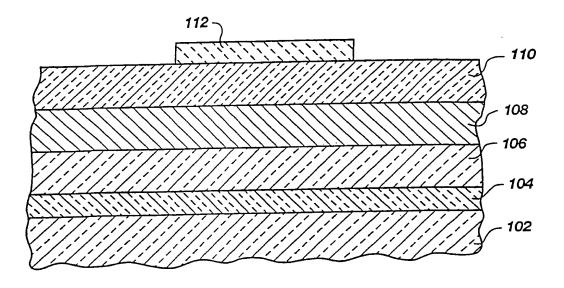


Fig. 5

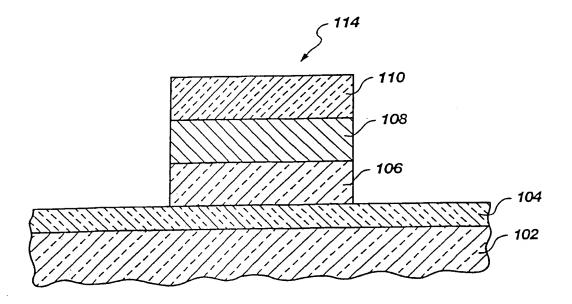
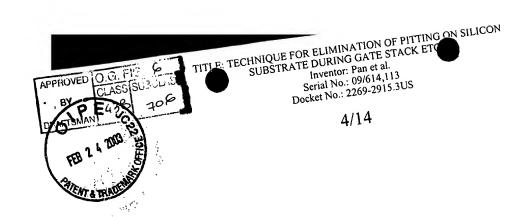
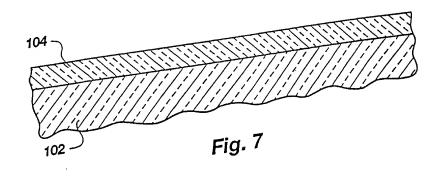
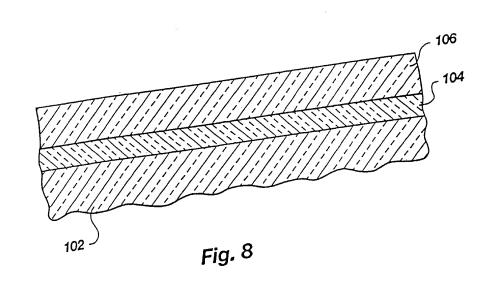
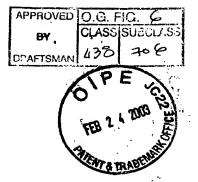


Fig. 6









TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON SUBSTRATE DURING GATE STACK ETC Inventor: Pan et al.
Serial No.: 09/614,113
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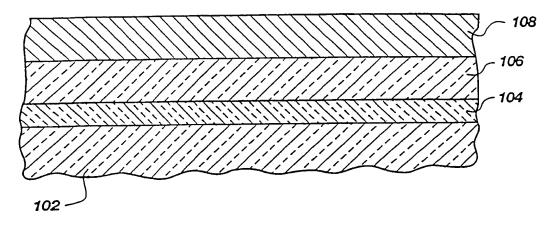


Fig. 9

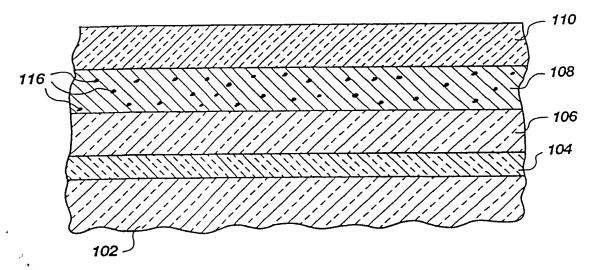


Fig. 10

APPROVED O.G. FIG. 6

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DPAFTSMAN 438 706

TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON SUBSTRATE DURING GATE STACK F

Inventor: Pan et al. Serial No.: 09/614,113 Docket No.: 2269-2915.3US



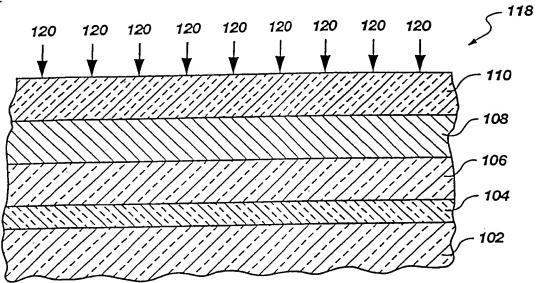


Fig. 11

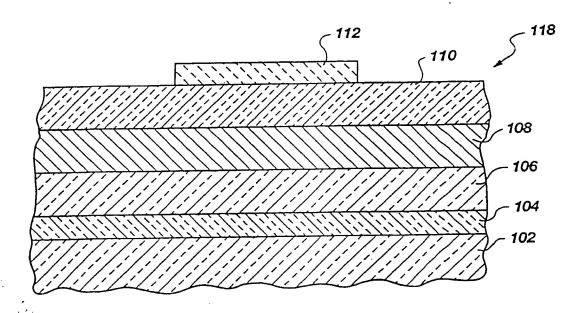


Fig. 12



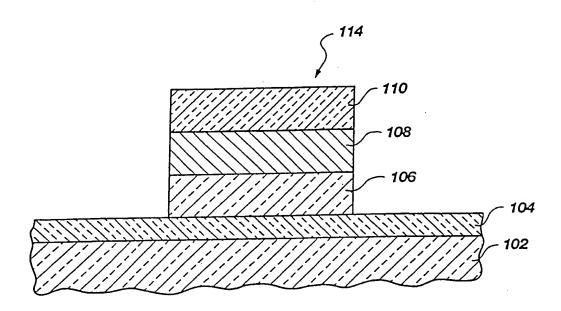


Fig. 13

APPROVED O.G. Fla. 6 BY DPAFTSMAN

TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON SUBSTRATE DURING GATE STACK ET Inventor: Pan et al.

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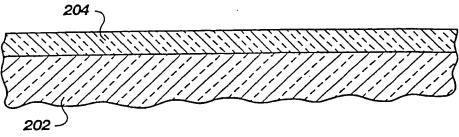
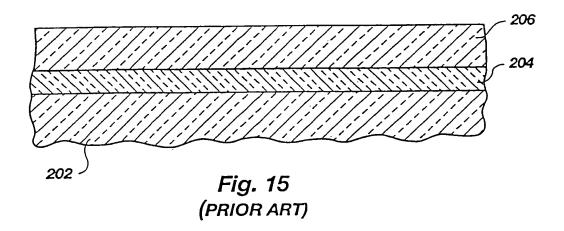
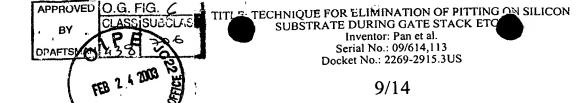


Fig. 14 (PRIOR ART)





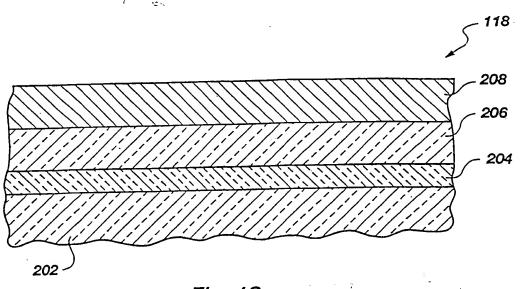


Fig. 16 (PRIOR ART)

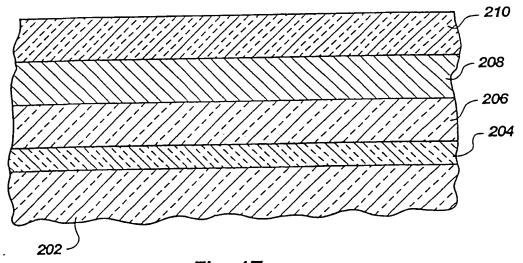


Fig. 17 (PRIOR ART)



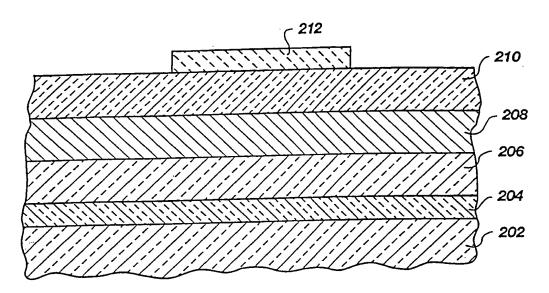


Fig. 18 (PRIOR ART)

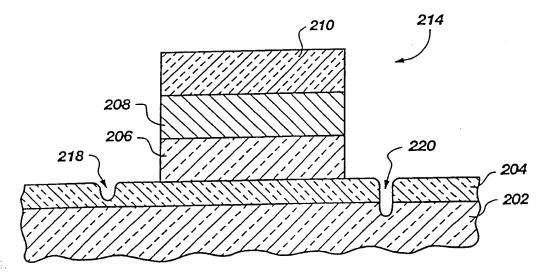


Fig. 19 (PRIOR ART)

SUBSTRATE DURING GATE STACK ET Inventor: Pan et al.
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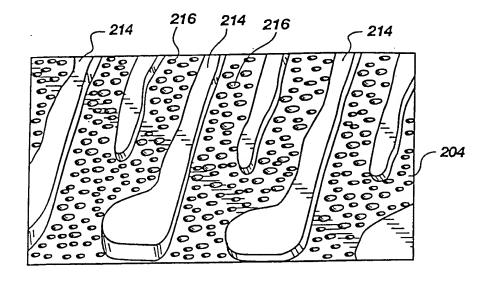


Fig. 20 (PRIOR ART)

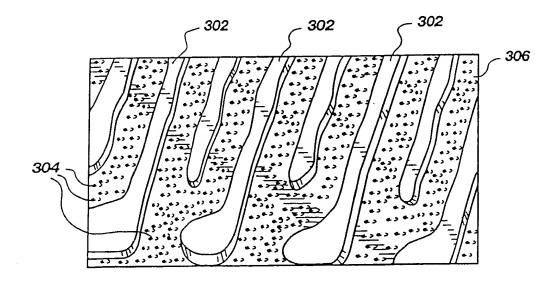
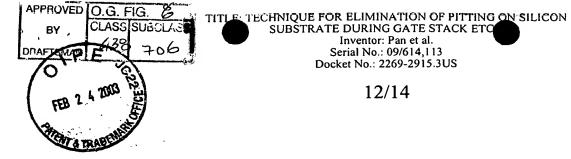


Fig. 21 (PRIOR ART)



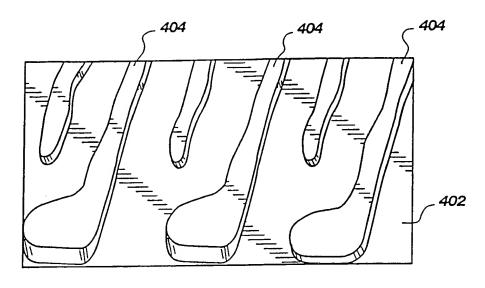


Fig. 22

APPROVED O.G. FIG. 6
CLASS SUBCLASS 438 706 DPAFTSMAN

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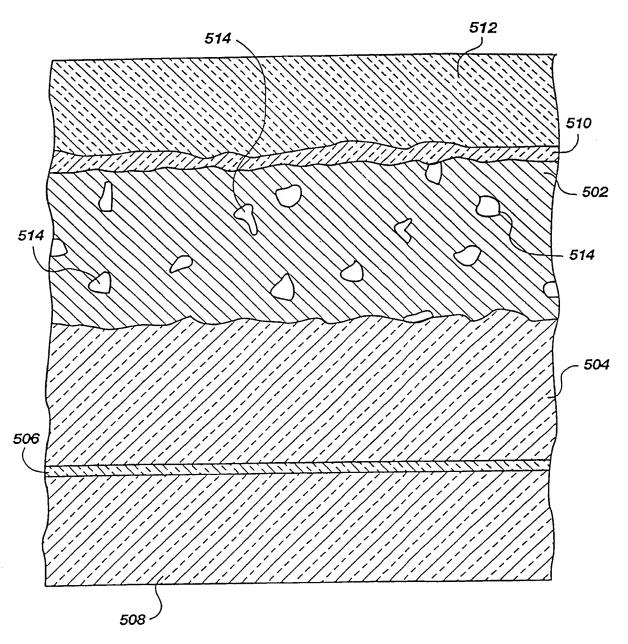


Fig. 23 (PRIOR ART)

APPHOVED O.G. FIG.

CLASS SUBCLASS

TITLE TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON SUBSTRATE DURING GATE STACK ETC

Inventor: Pan et al.

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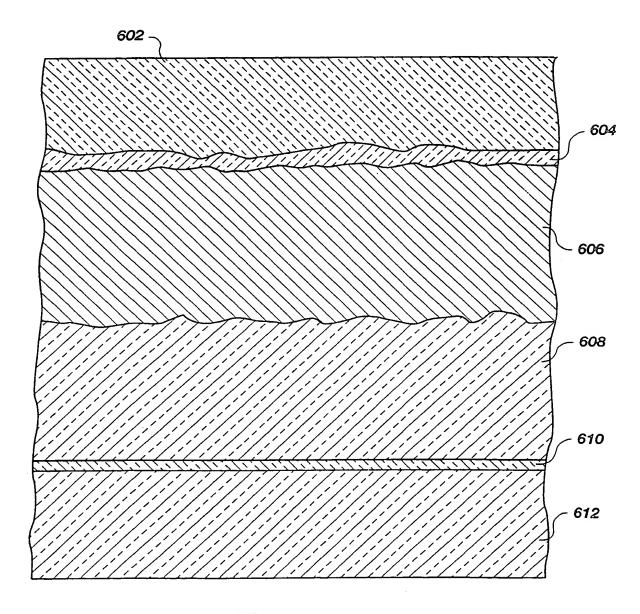


Fig. 24